

Claims

That which is claimed:

1. An integrated circuit memory device, comprising:
a source line;
a data input circuit that is operative to output an n bit data word;
a dummy data input circuit that is operative to output a complement of the n
5 bit data word;
a memory cell array that comprises n memory cells that are connected to the
source line, the n memory cells being operative to draw current from the source line
responsive to the n bit data word; and
a dummy memory cell array that comprises n dummy memory cells that are
connected to the source line, the n dummy memory cells being operative to draw
current from the source line responsive to the complement of the n bit data word such
that a total number of memory cells and dummy memory cells drawing current from
10 the source line is n.
2. The integrated circuit memory device of Claim 1, wherein each of the n
memory cells and the n dummy memory cells is a split-gate flash memory cell.
- 15 3. The integrated circuit memory device of Claim 1, wherein the n
memory cells and the n dummy memory cells are commonly connected to the source
line by respective source terminals.
4. The integrated circuit memory device of Claim 1, wherein the n
20 memory cells are connected to the n bit data word via n drain terminals, respectively,
and wherein the n dummy memory cells are connected to the complement of the n bit
data word via n dummy drain terminals, respectively.
5. An integrated circuit memory device, comprising:
25 a source line;

a memory cell array that comprises n memory cells that are connected to the source line, the n memory cells being operative to draw current from the source line responsive to an n bit data word; and

a dummy memory cell circuit that is operative to draw current from the source line responsive to the n bit data word such that a total current drawn by the memory cell array and the dummy memory cell circuit during a program operation is given by $n * a$ current drawn by one of the n memory cells.

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6. The integrated circuit memory device of Claim 5, wherein each of the n memory cells is a split-gate flash memory cell.

7. The integrated circuit memory device of Claim 5, wherein the n memory cells are commonly connected to the source line by respective source terminals.

8. The integrated circuit memory device of Claim 5, further comprising:
a data input circuit that generates n output voltages in response to the n bit data word; and
wherein the n memory cells receive the n output voltages via n drain terminals, respectively.

9. The integrated circuit memory device of Claim 5, wherein the dummy memory cell circuit comprises:
a current adding circuit that generates an output voltage on a dummy bit line in response to the n bit data word; and
a dummy memory cell that is operative to draw current from the source line responsive to the output voltage on the dummy bit line.

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10. An integrated circuit memory device, comprising:
a source line;

a memory cell array that comprises n memory cells that are connected to the source line, the n memory cells being operative to draw current from the source line responsive to an n bit data word; and

a dummy memory cell circuit that comprises n/y dummy memory cells that are connected to the source line, the n/y dummy memory cells being operative to draw current from the source line responsive to the n bit data word such that respective currents drawn by respective ones of the n/y dummy memory cells ranges from
5 approximately zero to $y * a$ current drawn by one of the n memory cells.

11. The integrated circuit memory device of Claim 10, wherein each of the n memory cells and the n/y dummy memory cells is a split-gate flash memory cell.

10 12. The integrated circuit memory device of Claim 10, wherein the n memory cells are commonly connected to the source line by respective source terminals.

13. The integrated circuit memory device of Claim 10,
15 a data input circuit that generates n output voltages in response to the n bit data word; and

wherein the n memory cells receive the n bit data word via n drain terminals, respectively.

20 14. The integrated circuit memory device of Claim 10, wherein the dummy memory cell circuit comprises:

an input circuit that generates an output voltage on at least one dummy bit line in response to the n bit data word; and

a dummy memory cell array that comprises at least one dummy memory cell
25 that is operative to draw current from the source line responsive to the output voltage on the at least one dummy bit line.

15. A method of operating an integrated circuit memory device, comprising:

applying n programming voltages to a memory cell array that comprises n memory cells so as to cause the memory cell array to draw current from a source line; and

5 applying at least one programming voltage to a dummy memory cell circuit so as to cause the dummy memory cell circuit to draw current from the source line such that a total current drawn by the memory cell array and the dummy memory cell array during a program operation is given by $n \times$ a current drawn by one of the n memory cells.

10 16. The method of Claim 15, further comprising:
generating the n programming voltages in response to an n bit data word; and
generating the at least one programming voltage in response to the n bit data word.

15 17. A flash memory device, comprising:
a memory cell array including $n_i \times 2^m$ memory cells having a drain connected to each of n_i bit lines in which each of n groups of memory cells comprises i bit lines, a gate connected to each of 2^m word lines, and a source connected to each of m source lines; and

20 a dummy array including 2^m transistors having a gate connected to each of the 2^m word lines, a source connected to each of the m source lines, and a drain connected to at least one or more dummy bit line;

 wherein in a program operation, a sum of a bias current flowing from the source line to the bit lines and a bias current flowing from the source line to the at
25 least one or more dummy bit line in response n input data is identical to a bias current flowing from the source line to the n bit lines when the n memory cells in the memory cell array are programmed.

 18. A flash memory device, comprising:
30 a memory cell array including $n_i \times 2^m$ memory cells having a drain connected to each of n_i bit lines in which each of n groups of memory cells comprises i bit lines, a gate connected to each of 2^m word lines, and a source connected to each of m source lines;

a program circuit that is operable to generate a bias current flow from a selected source line to selected bit lines of the memory cell array in response to n input data in a program operation;

5 a dummy array including $2m$ transistors having a gate connected to each of the $2m$ word lines, a source connected to each of the m source lines, and a drain connected to at least one dummy bit lines; and

a dummy program circuit that is operable to generate a bias current flow from a selected source line of the dummy array to the at least one or more dummy bit lines in response to the n input data in a program operation.

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19. The device of Claim 18, wherein in a program operation, a sum of a bias current flowing from the selected source line to the selected bit lines and a bias current flowing from the selected source line to the at least one or more dummy bit lines is identical to a bias current flowing from the selected source line to the n bit lines when n memory cells in the memory cell array are programmed.

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20. The device of Claim 18, wherein each of the $n \times 2m$ memory cells is a split-gate flash memory cell.

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21. The device of Claim 18, wherein the dummy array comprises $n \times 2m$ dummy memory cells having a drain connected to each of the n dummy bit lines, a gate connected to each of the $2m$ word lines and a source connected to each of the m source lines.

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22. The device of Claim 21, wherein each of the $n \times 2m$ dummy memory cells is a split-gate flash memory cell.

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23. The device of Claim 21, wherein the dummy program circuit comprises n data input circuits inputting data to each of the n dummy bit lines in response to the n input data;

each of the n data input circuits comprising:

a first pull-up transistor having a source to which a power voltage is applied, a gate to which the input data is applied, and a drain connected to the dummy bit line;

a first pull-down transistor having a drain connected to the dummy bit line and a gate to which the input data is applied;

a bias current generating transistor having a drain connected to a source of the first pull-down transistor and a source to which a ground voltage is applied and
5 generating the bias current flow in response to a bias voltage generated in a program operation; and

a reset transistor resetting the dummy bit line to a ground voltage level in response to a control signal generated in an erase operation, a read operation, and a standby condition.

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24. The device of Claim 18, wherein the dummy array comprises $n/y \times 2m$ dummy memory cells having a drain connected to each of n/y dummy bit lines, a gate connected to each of the $2m$ word line, and a source connected to each of the m source lines.

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25. The device of Claim 24, wherein each of the $n/y \times 2m$ dummy memory cells is a split-gate flash memory cell.

26. The device of Claim 24, wherein the dummy program circuit comprises
20 n/y groups of data input circuits providing data to each of the n/y dummy bit lines in response to a predetermined number of input data of the n input data,

each of the n/y groups of the data input circuits comprises:

an OR gate that is operable to perform a logical OR of the predetermined number of the input data;

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a first pull-up transistor having a source to which a power voltage is applied, a gate to which an output signal of the OR gate is applied, and a drain connected to the dummy bit line;

a predetermined number of first pull-down transistors having a drain connected to the dummy bit line and a gate to which the predetermined number of the
30 input data is respectively applied;

a predetermined number of bias current generating transistors having a drain connected to a source of each of the predetermined number of the first pull-down

transistors and a source to which a ground voltage is applied and generating the bias current flow in response to a bias voltage generated in a program operation; and

a reset transistor resetting the dummy bit line to a ground voltage level in response to a control signal generated in an erase operation, a read operation and a standby condition.

27. The device of Claim 18, wherein the dummy array comprises $2m$ transistors having a drain connected to one of the at least one dummy bit line, a gate connected to each of the $2m$ word lines, and a source connected to each of the m source lines.

28. The device of Claim 27, wherein each of the $2m$ transistors is an NMOS transistor, and a gate oxide of each of the NMOS transistors is relatively thick.

29. The device of Claim 27, wherein the dummy program circuit comprises a pull-up transistor having a source connected to the one of the at least one dummy bit line and a gate to which a combination signal of the n input data is applied; n pull-down transistors having a drain connected to a drain of the pull-up transistor and a gate to which the n input data are respectively applied;

n bias current generating transistors having a drain connected to a source of each of the n pull-down transistors, a gate to which a bias voltage is applied in a program operation, and a source to which a ground voltage is applied; and

a reset transistor operable to reset the dummy bit line to a ground voltage level in response to a control signal in an erase operation, a read operation, and a standby condition.

30. A method of programming a flash memory device, the flash memory device having a memory cell array including $n \times 2m$ memory cells having a drain connected to each of n_i bit lines in which each of the n groups of memory cells comprises i bit lines, a gate connected to each of $2m$ word lines, and a source connected to each of m source lines, the method comprising:

providing at least $2m$ transistors having a gate connected to each of the $2m$ word lines, a source connected to each of the m source lines, and a drain connected to at least one or more dummy bit lines;

5 generating a bias current from a selected source line of the memory cell array to $(n-x)$ selected bit lines in response to n input data in a program operation, where x is an integer from 0 to n ;

10 generating, in a program operation, a bias current flowing from the selected source line to the at least one or more dummy bit line in response to the n input data that is identical to a bias current flowing from the selected source line to the x bit lines when the x memory cells in the memory cell array are programmed.